P 44130 DE (5)

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 058 309 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
06.12.2000 Bulletin 2000/49

(51) Int Cl.7: **H01L 27/115**, H01L 29/788, H01L 21/8247

(21) Application number: **99830346.5**

(22) Date of filing: **04.06.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(71) Applicant: **STMicroelectronics S.r.l.**
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Dalla Libera, Giovanna**
  20052 Monza (IT)
- **Vajana, Bruno**
  24100 Bergamo (IT)
- **Patelmo, Matteo**
  20056 Trezzo sull'Adda (IT)

(74) Representative: **Cerbaro, Elena, Dr. et al**
STUDIO TORTA S.r.l.,
Via Viotti, 9
10121 Torino (IT)

(54) Process for manufacturing electronic devices comprising nonvolatile memory cells with dimensional control of the floating gate regions

(57) The manufacturing process comprises the steps of: forming a first insulating region (25b) on top of an active area; forming a tunnel region (98) laterally to the first insulating region; forming a floating gate region (95); sealing the floating gate region with an insulating region (96; 34); forming a control gate region (43b) on top of the floating gate region; and forming conductive regions (65a, 65b) in the active area (14). The floating gate region (95) is obtained by depositing and defining a semiconductor material layer (27) through a floating gate mask (90). The floating gate mask (90) has an opening (92) with an internally delimiting side (90b) extending at a preset distance from a corresponding externally delimiting side (90a) of the mask, and the semiconductor material layer (27) is removed laterally at the external and internal delimiting sides so that the tunnel area (98) is defined, as regards its length, by the floating gate mask alone.

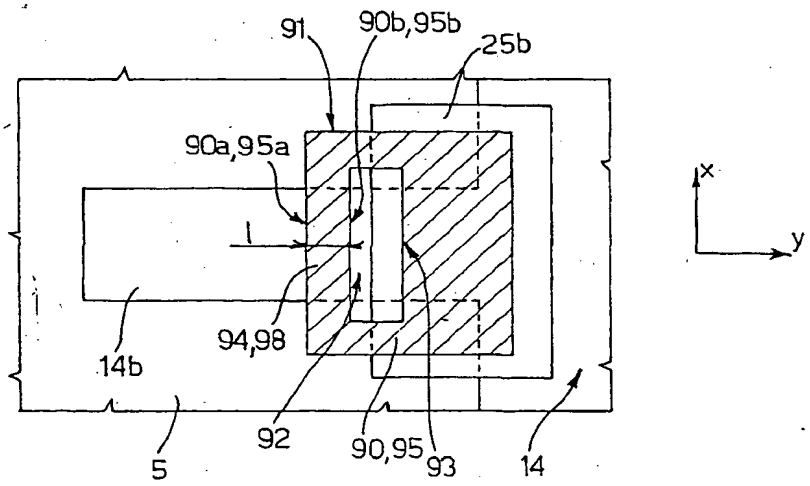


Fig. 27

EP 1 058 309 A1

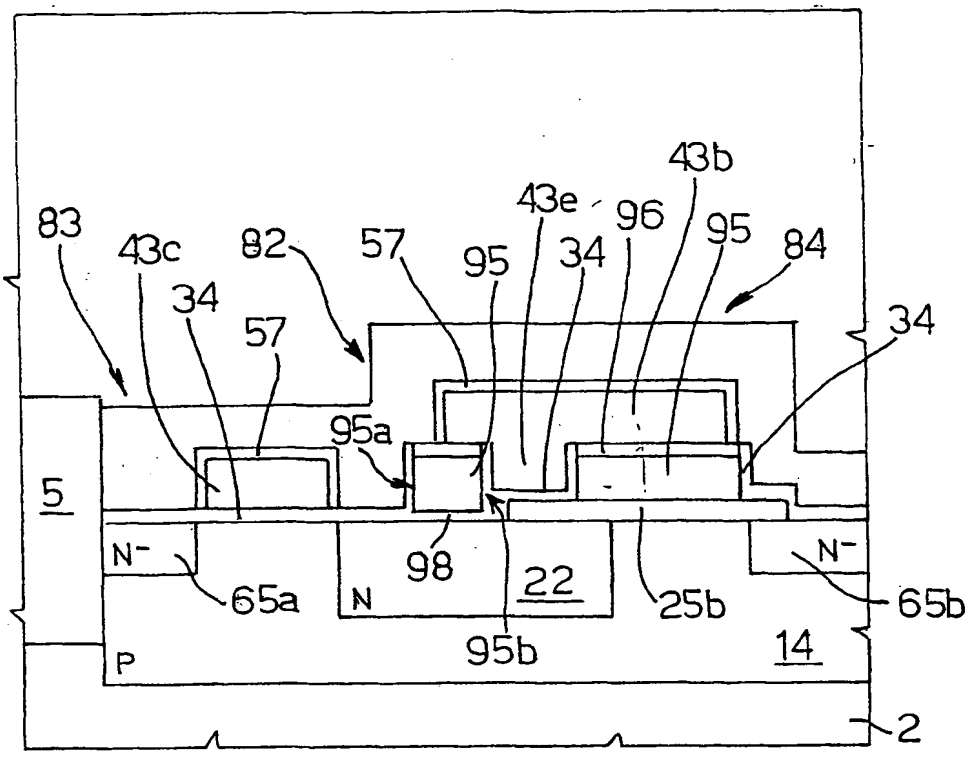

83
43c
34
82
57
57
95
43e
34
96
43b
95
84
34
95a
5
N⁻
65a
98
N
22
25b
N⁻
65b
P
95b
14
2

Fig. 29

Description

[0001] The present invention regards a process for manufacturing electronic devices comprising nonvolatile memory cells with dimensional control of the floating gate regions.

[0002] Devices using nonvolatile memories of the EEPROM type, such as smart cards, complex microcontrollers and mass storage devices requiring programmability of the single byte, call for increasingly higher levels of performance and reliability.

[0003] In practice, from the technological standpoint, this means that it is necessary to get high levels of performance (i.e., increasingly thinner tunnel oxides, ever more reduced programming voltages, increasingly greater current driving capability of the cells) to coexist with an extremely high reliability: one hundred thousand programming cycles and retention of the stored charge for at least ten years are by now considered the minimum requisites for the acceptance of this type of product on the market.

[0004] According to the above, it is necessary to develop new manufacturing processes and new geometries that are able to eliminate some of the critical aspects typical of memories, thus increasing their intrinsic reliability without reducing their performance, both for embedded applications (i.e., wherein the memory cells are associated to special electronic devices) and for stand-alone applications (i.e., wherein the device is merely a nonvolatile memory).

[0005] The purpose of the present invention is therefore to provide a manufacturing process that enables the critical aspects of known processes to be reduced.

[0006] According to the present invention, there are provided a process for manufacturing electronic devices comprising nonvolatile memory cells and an electronic device comprising nonvolatile memory cells, as defined in Claim 1 and Claim 9, respectively.

[0007] To help understanding of the present invention, a preferred embodiment is now described, purely by way of non-limiting example, with reference to the attached drawings, in which:

- figure 1 shows a cross-section of a silicon wafer in a first step of a known production method;
- figure 2 is a plan view of the wafer of figure 1;
- figures 3-7 show cross-sections similar to that of figure 1, in successive production steps;
- figure 8 is a plan view of the wafer of figure 7;
- figures 9-11 show cross-sections similar to that of figure 7, in successive production steps;
- figure 12 is a plan view of the wafer of figure 11;
- figures 13-17 show cross-sections similar to that of figure 11, in successive production steps;
- figure 18 is a plan view of the wafer of figure 17;
- figures 19-21 show cross-sections similar to that of figure 17, in successive production steps;
- figure 22 is a plan view of the wafer of figure 21;
- figures 23-25 show cross-sections similar to that of figure 21, in successive production steps;
- figure 26 shows a cross-section through a silicon wafer, in a step of the method according to the invention, for a portion of the wafer housing a memory cell, in enlarged scale;
- figure 27 shows a cross-section similar to that of figure 26;
- figure 28 and 29 show cross-sections similar to that of figure 26, in successive production steps;
- figures 30 and 31 show cross-sections in two subsequent steps for a different embodiment of the invention;
- figure 32 is a plan view showing part of the masks used in the different embodiment of the process according to the invention; and
- figure 33 shows a cross-section, similat to Figure 31, in a final manufacturing step of a different embodiment of the invention.

[0008] To help understanding of the present invention, a production method subject of European patent application 98830644.5, filed on 23.10.1998 in the name of the same applicant, is initially described with reference to figures 1 to 25. In detail, this method makes it possible to produce a device comprising LV (low-voltage and high-speed) and HV (high-voltage) NMOS transistors, LV and HV PMOS transistors, and EEPROM memory cells formed by a selection transistor and a memory transistor.

[0009] In particular, owing to the duality in forming NMOS and PMOS transistors, the drawings show only the steps for NMOS transistors, and the steps for forming PMOS transistors are described in words alone. The EEPROM memory cells form a memory array, and are produced in a part of the wafer thereafter also designed matrix area 15.

[0010] In figure 1, a wafer 1 formed by a monocrystalline silicon substrate 2, here of P type, has been subjected to the active area definition steps. In detail, with the surface 3 of the substrate 2 covered by an active area mask 4 of non-oxidisable material (typically of a double layer of silicon oxide and silicon nitride, defined using resist), wafer 1 has been subjected to thermal oxidation; consequently, in the parts of the substrate 2 not covered by the active area mask 4, a thick oxide layer (field oxide 5) has been grown, delimiting between each other active areas of the substrate, designed to accommodate various components of the device to be produced. In particular, figure 1 shows three active areas, i.e. a LV active area 6, designed to accommodate a LV NMOS transistor, an HV active area 7, designed to accommodate an HV NMOS transistor, and an active matrix area 8, designed to accommodate EEPROM memory cells.

[0011] In detail, and in a known manner, the active matrix area 8 defines a grid, of which figure 2 shows in full only the part relative to one cell, indicated at 9, hav-

ing substantially the shape of a "T" rotated by 90°, and comprises a leg 9a and a cross-piece 9b. The leg 9a is adjacent to, and electrically connected to, respective legs 9a of other cells arranged above and below the shown cell, of which only parts are visible; in addition, the leg 9a is connected to a leg of an adjacent cell to the right (not shown), which has a symmetrical structure with respect to that shown. The legs 9a are designed to accommodate source regions of the memory transistors; the end of the cross-pieces 9b not connected to the legs 9a is designed to accommodate drain regions of the selection transistors, and the gate regions of the cells must be provided on the cross-pieces 9b. Further active areas are generally provided for forming LV or HV PMOS transistors, not shown in the drawings.

[0012] Subsequently, the active area mask 4 is removed, the free surface 3 of the substrate is oxidated to form a sacrificial oxide layer 10, and doping ions of N type are implanted through a mask, for forming N-HV regions (not shown) for the HV PMOS transistors; using an HV P-well resist mask 11, covering the entire surface of wafer 1, except active HV area 7 and matrix area 8, doping ions of P type are implanted, as shown schematically in figure 3 by arrows 12. In the substrate 2, P-HV regions 13 of P type for high-voltage transistors, and a P-matrix region 14, also of P type, for the cells are then formed, as shown in figure 3. The P-HV regions 13 and P-matrix regions 14 reproduce exactly the shape of the active HV area 7 and matrix area 8, and thus, for each cell, legs 14a (corresponding to legs 9a of active cell areas 9, see figure 8), and cross-pieces 14b (figure 8, corresponding to cross-pieces 9b) are defined.

[0013] After removing the HV P-well mask 11, doping ions of N type are implanted through a mask for forming N-LV regions (not shown) for the LV PMOS transistors; then, using a LV P-well resist mask 17 covering the entire surface of the wafer 1, except active LV areas 6, doping ions of P type are implanted, as shown schematically in figure 4, by arrows 18. In the substrate 2, P-LV regions 19 of P type for the LV NMOS transistors are then formed, as shown in figure 4. Thereby, the P-HV region 13 and the P-LV regions 19 are separated from one another, and their electrical characteristics can be optimised with respect to the electrical characteristics required.

[0014] After removing the LV P-well mask 17, a capacitor mask 20 is formed, covering the entire surface of wafer 1, except strips perpendicular to cross-pieces 14b. Doping ions of N type (for example phosphorous) are then implanted, as shown schematically in figure 5 by arrows 21. In the cross-pieces 14b, continuity regions 22, of N type, are then formed, as necessary for electrical continuity between each selection transistor and the respective memory transistor of each cell. The structure of figure 5 is then obtained.

[0015] After removing the capacitor mask 20, the wafer 1 is subjected to annealing, the sacrificial layer 10 is removed, and matrix oxidation is carried out, forming a matrix oxide layer 25 on the surface of all regions 13, 14, and 19. Then, using a matrix oxide mask 24, shown in cross-section in figure 7 and in plan view in figure 8, the matrix oxide is removed from everywhere except from beneath the matrix oxide mask 24, forming a region 25b in the P-matrix region 14 that is partially arranged above the continuity region 22, and partially covers the leg 9a, and a masking region 25a on the P-LV region 19 (figure 7).

[0016] After removing the matrix oxide mask 24, wafer 1 is oxidised again, forming a tunnel oxide layer 26 on the entire surface of the substrate, where the latter is exposed, and increasing the thickness of the oxide that is already present (regions 25a, 25b) in regions 14 and 19. The structure of figure 9 is thus obtained.

[0017] A first polycrystalline silicon layer is then deposited (poly1 layer 27), which is suitably doped; subsequently, an interpoly dielectric layer 31 is formed, for example of a triple layer of ONO (silicon oxide-silicon nitride-silicon oxide), as shown in figure 10.

[0018] A floating gate mask 30 shown in figure 11 and 12 is then formed; dielectric layer 31, poly1 layer 27, and tunnel oxide layer 26 are then etched everywhere except where the floating gate regions of the memory transistors are to be formed, indicated at 27b in figure 11; consequently, of the tunnel oxide layer 26, only a tunnel region 26b is left, adjacent to an edge of the floating gate region 27b of the memory transistor. In this step, the thickness of the region 25a decreases again on the active area 19.

[0019] After removing the floating gate mask 30, an HV oxidation step is carried out, forming an HV gate oxide layer 34 on the entire free surface of substrate 2, in particular on P-HV regions 13 and P-matrix regions 14 (figure 13). Portions of oxide 34 are also formed laterally to the floating gate region 27b of the memory transistor, as shown in figure 13, and the thickness of the region 25a increases again. Subsequently, using an HV oxide resist mask 35, which covers the P-HV region 13 and the matrix area 15, the region 25a is removed from above the P-LV regions 19 (figure 14).

[0020] After removing the HV oxide mask 35, a LV oxidation step is carried out, forming a LV gate oxide layer 36 above the P-LV regions 19; in addition, the thickness of the HV gate oxide layer 34 increases above the P-HV region 13 and the P-matrix regions 14, thus providing the structure of figure 15.

[0021] Then a second polycrystalline layer (non-doped poly2 layer 43) is deposited, as shown in figure 16. A LV gate mask 44 is formed, covering the N-HV regions (not shown), the P-HV regions 13, and the matrix area 15. In addition, the LV gate mask 44 covers the poly2 layer, above the P-LV regions 19, where both the NMOS and PMOS gate regions of the LV transistors must be defined, as shown in figures 17 and 18, and above the N-LV regions (not shown) where the gate regions of the LV PMOS transistors must be defined. The exposed portions of the poly2 layer 43 are removed,

thus providing the structure of figure 17, wherein the portions of poly2 remaining above P-LV regions 19 form gate regions 43a of the LV NMOS transistors. As can be seen, during the step of defining the gate regions of the LV transistors, the layers above the P-HV regions 13 and P-matrix regions 14 are protected, as are the layers above the N-HV regions (not shown); consequently, the method described provides separate definition of the gate regions of the LV transistors and HV transistors, as well as of the memory cells.

[0022] After removing the LV gate mask 44, and re-oxidation, to seal the gate regions 43a of the LV NMOS transistors, using a resist mask not shown, which covers the N-LV and N-HV regions, doping ions of N type are implanted (LDDN implanting), as schematised in figure 19 by arrows 47. Laterally on the gate regions 43a (inside the P-LV regions 19), LDD regions 48 of N type are then formed; in addition, the poly2 layer 43 is suitably doped.

[0023] After removing the resist mask, not shown, masked implanting of doping ions of P type is carried out; in particular, during this step, the P-HV 13 regions and P-LV 19 regions, as well as the matrix region 15, are covered, whereas in the N-LV regions, LDD regions of P type (not shown) are formed. On the entire surface of the wafer 1, a dielectric layer (for example TEOS - TetraEthylOrthoSilicate) is then deposited; then, in a known manner, the TEOS layer is subjected to anisotropic etching, therefore it is removed completely from the horizontal portions, and remains laterally to the gate regions 43a, where it forms spacers 52, and partially on the floating gate regions 27b, on the matrix area 15 (figure 20). On the other hand, spacers are not formed above the field oxide regions 5, owing to the bird's beak shape of the latter (in a known manner, not shown for simplicity); furthermore, spacers are not formed above the P-HV regions 13 and the respective N-HV regions, since the gate regions of the HV transistors are not yet defined.

[0024] Subsequently, using a resist mask not shown, which covers the N-LV and N-HV regions, doping ions of N type are implanted, as schematised in figure 20 by arrows 54. LV-NMOS source and drain regions 55 of N+ type are then formed in the P-LV regions 19, in a self-aligned manner with the spacers 52. The LV-NMOS source and drain regions 55 are more highly doped than the LDD regions 48. In addition, the poly2 layer 43 and the gate regions 43a are doped N type, whereas the areas where HV and LV PMOS transistors are to be produced are covered. The structure of figure 20 is thus obtained.

[0025] After removing the resist mask (not shown), a similar step of masked implanting doping ions of P type is carried out, for forming respective source and drain regions in the N-LV regions (in a not shown manner), and for doping P type the poly2 layer 43, above the N-LV and N-HV regions. In this step, the P-LV regions 19, P-HV regions 13, and P-matrix region 14, are completely covered.

[0026] Subsequently, an HV gate mask 56 is formed, which covers the surface of the wafer 1, with the exception of the active areas where the gate regions of the high-voltage transistors are to be formed (P-HV regions 13, in the case of HV NMOS), and the portions of the P-matrix region 14 designed to form the gate regions of the selection transistor, and the control gate regions of the memory transistors (in this respect see figures 21 and 22). Then, the portions of poly2 layer 43 not covered by the HV gate mask 56 are etched; the structure of figure 21 is thus obtained.

[0027] Subsequently, re-oxidation is carried out, forming an oxide layer 57 on the entire free surface of substrate 2, in particular laterally on the floating gate regions 27b and control regions 43b of the memory transistors, and laterally on the gate regions of the selection transistors, as shown in figure 23, wherein the gate region of the selection transistor is indicated at 43c, the gate region of the memory transistor is indicated at 43b, and the gate region of the HV NMOS transistor is indicated at 43d.

[0028] After removing the HV gate mask 56 and re-oxidation, an NHV mask, not shown, is formed, covering N-LV and N-HV regions (not shown). Using the NHV mask, doping ions of N type are implanted, as shown schematically in figure 23 by arrows 63. In P-HV regions 13, at both sides of HV gate regions 43d, HV-NMOS source and drain regions 64 of N type are then formed, less doped than LV-NMOS source and drain regions 55; simultaneously, in the P-matrix region 14, drain regions 65a of selection transistor are formed, on one side, in a self-aligned manner with the gate regions 43c of the selection transistors, and the source regions 65b of the memory transistor are formed on the side not facing the respective selection transistor, in a aligned manner with the gate region 43b of the memory transistors. In addition, the areas arranged between each selection transistor and the respective memory transistor are also implanted; however, this implanting generally takes place inside the continuity regions 22, more doped, and is therefore not shown (for this reason the respective area is represented with broken lines). However, in case of misalignments, this implanting guarantees electrical continuity. The HV-NMOS source and drain regions 64 of the HV selection transistor 65a, and the source regions 65b of the memory transistor (as well as the regions) have a lower doping level than the LV-NMOS source and drain regions 55, and thus have a higher breakdown voltage and higher resistivity.

[0029] After removing the NHV mask, the source and drain regions of the HV PMOS transistors (not shown) are similarly implanted using a mask.

[0030] Subsequently a protection dielectric layer 70, for example of TEOS or nitride, is deposited on the entire surface of the wafer 1. A salicide protection mask 72, shown in figure 24, is then formed, covering the surface of wafer 1, except the active areas where the low-volt-

age transistors are formed (P-LV regions 19, for the NMOS). Using the salicide protection mask 72, dielectric layer 70 is removed from above the P-LV regions 19 (figure 24). After removing the salicide protection mask 72, if zener diodes, low-doping precision resistors, and/or transistors of N and P type with non-salicided junctions are to be formed, a dielectric layer is deposited and defined using a suitable mask, in a not shown manner. Otherwise, the uncovered poly2 layer are immediately salicided. Saliciding, carried out in a known manner, as previously described, causes titanium silicide regions to form above the source and drain regions of the LV NMOS and PMOS transistors (silicide regions 75a1 above the LV-NMOS source and drain regions 55, and similar regions for the LV PMOS transistors), above the gate regions of the LV NMOS and PMOS transistors (silicide regions 75a2 above the gate regions 43a for the LV NMOS transistors, and similar regions for the LV PMOS transistors), as shown in figure 25.

[0031] After forming a protection dielectric layer 78, the final structure of figure 25 is obtained, showing an LV NMOS transistor 80, an HV NMOS transistor 81, and an EEPROM cell 82, formed by a selection transistor 83 and a memory transistor 84. The final steps follow, including forming contacts and electrical interconnection lines, deposition of a passivation layer, etc.

[0032] In the described process, the problem exists that the length of the tunnel area in the horizontal direction of the cross section of Figure 25, which is equal to the length of the tunnel region 26b, is determined by two different masks, since the left edge of the tunnel region 26b in Figure 25 is defined by the floating gate mask 30, and the right edge of the tunnel region 26b, delimited by the matrix oxide region 25b, is defined by the matrix oxide mask 24, as is evident from Figure 11. Consequently, the inevitable misalignments between the two masks 24 and 30 affect the dimensions of the tunnel area in the horizontal direction of Figure 25. The lack of a precise dimensional control over the tunnel area thus determines a critical situation and a reduction in reliability.

[0033] In addition, the above mentioned misalignments determine different variations in the dimensions of the adjacent cells. In fact, in a memory array of the described type, adjacent cells (in the horizontal direction of the figures) are arranged alternately in a symmetrical way (in Figure 2, the adjacent cell to the right of the fully shown cell presents the leg 9a on the left and the cross-piece 9b on the right, whilst the subsequent cell has the same orientation as the shown cell). Consequently, the above misalignment between the two masks towards the left or towards the right causes alternatively an increase of the length of the tunnel region 26b in one half of the cells and a reduction in the remaining half of the cells. It follows that the electrical characteristics of the memory cells are not uniform, but are of two different types, according to whether a particular cell is "even" or "odd", with a consequent reduction in the reliability of the memory array.

[0034] To solve the above problem, a new fabrication process is here proposed, and only the steps of the new fabrication different from the previous process are described.

[0035] In detail, the present fabrication process comprises the initial steps described with reference to Figures 1-10 until the interpoly dielectric layer 31 is formed.

[0036] Subsequently, the floating gate mask is formed having a different shape from that of the known process, as shown in Figures 26 and 27. In detail, in the top view of Figure 27, the floating gate mask, here indicated by 90, has an external perimetral edge 91 of a rectangular shape, a side 90a of which extends perpendicularly to the cross-piece 14b (parallel to the x axis in Figure 27), in an approximately central position with respect to the cross-piece 14b itself. The floating mask 90 has an opening 92 delimited by an internal perimetral edge 93. The internal perimetral edge 93 is also rectangular, and its sides are parallel to the sides of the external perimetral edge 91; in particular, a side 90b of the internal perimetral edge 93 facing the side 90a delimits, together with the side 90a itself, a mask portion 94 having a preset width $\underline{1}$ (y direction in Fig. 27) corresponding to the desired width for the tunnel area. The position of the floating gate mask 90 and the size of the opening 92 are chosen so that the left edge of the matrix oxide region 25b (facing the selection transistor, still to be made) falls within the opening 92 even in the event of misalignments, as will be explained in what follows. Preferably, the left edge of the matrix oxide region 25b is set roughly in the centre of the opening 92; moreover, the latter has, for example, a width of 0.5 μm (for a 0.35 μm process).

[0037] Subsequently, as in the prior process, the interpoly dielectric layer 31 and the polyl layer 27 are etched in succession. Because of the shape of the floating gate mask 90, here these layers are removed also internally, under the opening 92. Consequently, at the end of etching, the floating gate region, now indicated by 95, and the interpoly dielectric region, now indicated by 96, present the same rectangular holed shape as the mask 90. In particular, the sides of the floating gate region 95 corresponding to the externally delimiting edge 90a and the internally delimiting edge 90b, indicated by 95a and 95b, respectively, define the length of the tunnel area in the y direction, now determined solely by the dimensions of the floating gate mask 90, and namely by the length $\underline{l}$ of the mask portion 94.

[0038] The size of the tunnel area in the perpendicular direction (x direction in Figure 27) is instead determined, as in the prior process, by the width of the cross-piece 14b of the P-matrix region 14 (active area of the cell).

[0039] In Figure 28 and in the subsequent figures, the portion of the tunnel layer 26 delimited by the sides 95a and 95b of the floating gate region 95 and making up the tunnel region is indicated by 98.

[0040] The manufacturing process then comprises the previously described steps including a re-oxidation step for completely sealing the floating gate region 95

also inside the hole determined by the opening 92. In particular - see Fig. 28 - as for the prior process described previously, an HV gate oxide layer 34 is grown, joining with the layer 26, the dimensions whereof can be calibrated in a known way. Next, the second polycrystalline silicon layer (poly2 layer, 43) is deposited and fills the hole inside the floating gate region 95, as evident from Figure 28, where the filling region is indicated by 43e.

[0041] The further steps are then carried out for forming the gate region 43c of the selection transistor 83, forming the P-channel and N-channel HV and LV transistors, and forming the conductive regions 48, 55, 64, 65a, and 65b in the active areas. As regards the memory cell 82, the final structure shown in Figure 29 is thus obtained.

[0042] The thus described method makes it possible to control the dimensions of the tunnel area 98 with a precision which depends only upon the dimensional control of the active area mask 4 and floating gate mask 90, and not upon the misalignments between the masks, which are much harder to control.

[0043] In addition, given that the dimensions of the tunnel area 98 do not depend upon the misalignments, the variability of the dimensions of "even" cells and "odd" cells discussed above no longer exists, and hence the memory cells 82 present more uniform electrical characteristics.

[0044] The presence of the opening in the floating gate region 95 calls for appropriate re-sizing of the cell. In fact, on the one hand, the area of the floating gate region 95 of the sensing transistor 84 is reduced, and, on the other hand, the coupling surface between the floating gate region 95 and the control gate region 43b increases, on account of the coupling existing between the filling region 43a and the portions of the floating gate region 95 facing it. Consequently, the present memory cell requires, on the whole, a larger area than the prior cell, but presents better electrical characteristics; consequently it may be advantageously applied when the requisites of area occupied are less stringent (for example, but not only, in "embedded" applications), and where it is necessary to have high electrical characteristics and high reliability.

[0045] Finally, it is clear that numerous modifications and variations can be made to the method and to the electronic device described and illustrated herein, all of which falling within the scope of the invention, as defined in the attached claims. For example, the tunnel layer 26 may be etched or not during the definition of the floating gate region 95; in addition, instead of being completely inside the floating gate region 95, the hole 97 may face one side of the latter, perpendicular to the side 95b.

[0046] According to a different embodiment described hereinafter, the interpoly dielectric layer 31 may be deposited and defined in an own subsequent step, instead of together with the floating gate region 95. In detail, according to this different embodiment, initially the steps described for the prior process with reference to Figures 1-9 are carried out, up to depositing the first polycrystalline silicon layer 27. Subsequently, the interpoly dielectric layer 31 is not formed, but the floating gate mask 90 is immediately formed with the same shape as described above, as shown in Fig. 30 and, with top view, in Fig. 32.

[0047] An interpoly dielectric layer 101 is next formed, for example, comprising a triple ONO layer (silicon oxide-silicon nitride-silicon oxide). Then, using an ONO mask 110, indicated in Fig. 32 by the dashed-and-dotted line and having dimensions greater than the external dimensions of the floating gate mask 90, the interpoly dielectric layer 101 is removed everywhere, except above and at the sides of the floating gate region 95, so as to seal the floating gate region 95 completely also inside the hole 97, as shown in Fig. 31.

[0048] Next, the high voltage oxide layer 34 is grown, and the poly2 layer 43 is deposited. Then, subsequent steps are carried out for forming the gate region 43c of the selection transistor 83, forming the P-channel and N-channel HV and LV transistors, and forming the conductive regions 48, 55, 64, 65a, and 65b in the active areas. As regards the memory cell 82, the final structure shown in Fig. 33 is then obtained.

[0049] This embodiment has the advantage of insulating better the floating gate region 95, so that the resulting memory cell becomes more reliable.

Claims

1. A process for manufacturing electronic devices comprising floating gate nonvolatile memory cells (82), including the steps of:

   - defining an active area (14) in a substrate (2) of semiconductor material;
   - forming a first insulating region (25b) on top of said active area;
   - depositing a first dielectric material layer (26) on top of said substrate (2); said first dielectric material layer (26) comprising a tunnel area (98);
   - forming a floating gate region (95) on top of said first dielectric material layer (26) and on top of said first insulating region (25b);
   - forming a second insulating region (96, 34) surrounding said floating gate region;
   - forming a control gate region (43b) on top of said floating gate region; and
   - forming conductive regions (65a, 65b) in said active area (14);

   said step of forming a floating gate region (95) comprising the steps of depositing a first semiconductor material layer (27) on top of said dielectric material layer and selectively removing said first semicon-

ductor material layer using a floating gate mask (90) having an externally delimiting side (90a), characterized in that said floating gate mask (90) has an opening (92) having an internally delimiting side (90b) facing said externally delimiting side (90a) at a preset distance, and in that said step of selectively removing comprises the step of removing said first semiconductor material layer (27) laterally to said externally and internally delimiting sides (90a, 90b).

2. The process according to Claim 1, characterized in that said step of forming a floating gate region (95) comprises the step of forming a polygonal region having a hole (97).

3. The process according to Claim 1 or Claim 2, characterized in that said floating gate mask (90) has an external perimetral edge (91) of rectangular shape, in that said opening (92) has an internal perimetral edge (93) of rectangular shape, in that said externally delimiting side (90a) and said internally delimiting side (90b) are parallel to one another, facing one another, and delimit between each other a mask portion (94) defining a length dimension of said tunnel area (98).

4. The process according to any of Claims 1-3, characterized in that said opening (92) is arranged astride of or laterally to said first insulating region (25b).

5. The process according to any of Claims 2-4, characterized in that said step of forming a second insulating region (96, 34) comprises the steps of forming first sealing portions (96) covering a top surface, and second sealing portions (34; 96) covering at least side walls of said floating gate region (95) that delimit said hole (97), and in that said step of forming a control gate region (43b) comprises the steps of depositing a second semiconductor material layer (43), said second semiconductor material layer filling said hole (97) in said floating gate region (95).

6. The process according to Claim 5, characterized in that said step of forming a second insulating region (96, 34) comprises the steps of depositing a second dielectric material layer (96) on top of said first semiconductor material layer (27); selectively removing said second dielectric material layer (96) using said floating gate mask (90), obtaining said first sealing portions (96); and forming said second sealing portions (34).

7. The process according to Claim 5, characterized in that said step of forming a second insulating region comprises the steps of depositing a second dielectric material layer (96) on top of and at the sides of said floating gate region (95); and selectively removing said second dielectric material layer (96) from a surface of said substrate, laterally to said floating gate region (95), thus forming said first and second sealing portions (96).

8. The process according to any of Claims 1-7, characterized in that said cell (82) is an EEPROM cell and in that the process further comprises forming a selection transistor (83) to laterally to and at a distance from said tunnel region (98).

9. An electronic device (82) comprising a nonvolatile memory element (84) comprising a substrate (2) of semiconductor material housing an active region (14); conductive regions (65a, 65b) in said active area; a first insulating region (25b) on top of said active area; a tunnel region (98), of dielectric material, on top of said active area, laterally to said first insulating region (25b); a floating gate region (95) on top of said tunnel region and said first insulating region; a second insulating region (96, 34) surrounding said floating gate region; and a control gate region (43b) on top of said floating gate region; characterized in that said floating gate region (95) internally presents a hole (97); in that said second insulating region (96, 34) further extends on internally delimiting walls (95b) of said hole (97) and in that said control gate region (43b) comprises a filling portion (43e) extending in said hole.

10. The device according to Claim 9, characterized in that said floating gate region (95) has, in top view, an external perimetral edge (91) of rectangular shape having an externally delimiting side (95a), in that said hole (97) has, in top view, an internal perimetral wall (93) of rectangular shape having an internally delimiting side (95b) facing said externally delimiting side (95a) and parallel thereto.

11. The device according to Claim 10, characterized in that said nonvolatile memory element (84) belongs to an EEPROM cell (82) further comprising a selection transistor (83) arranged adjacent to and at a distance from said nonvolatile memory element and facing said tunnel region (98).

Fig.1

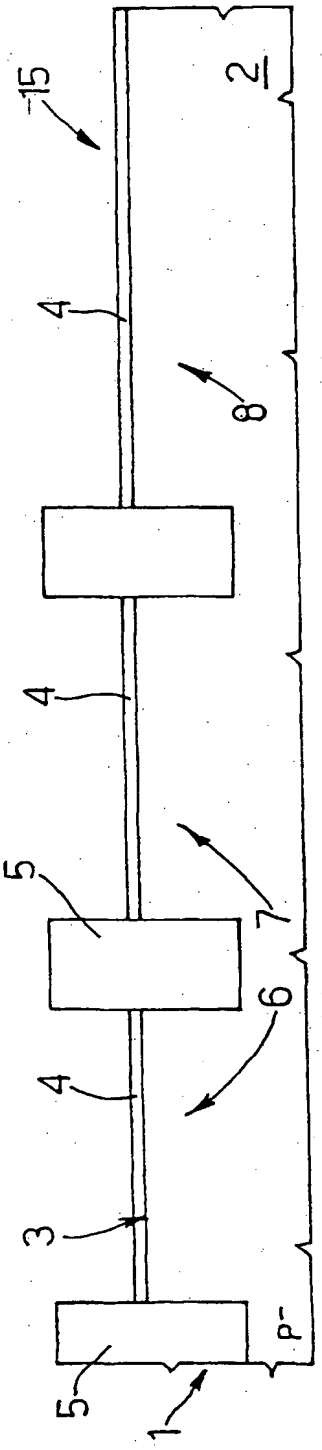


Fig.2

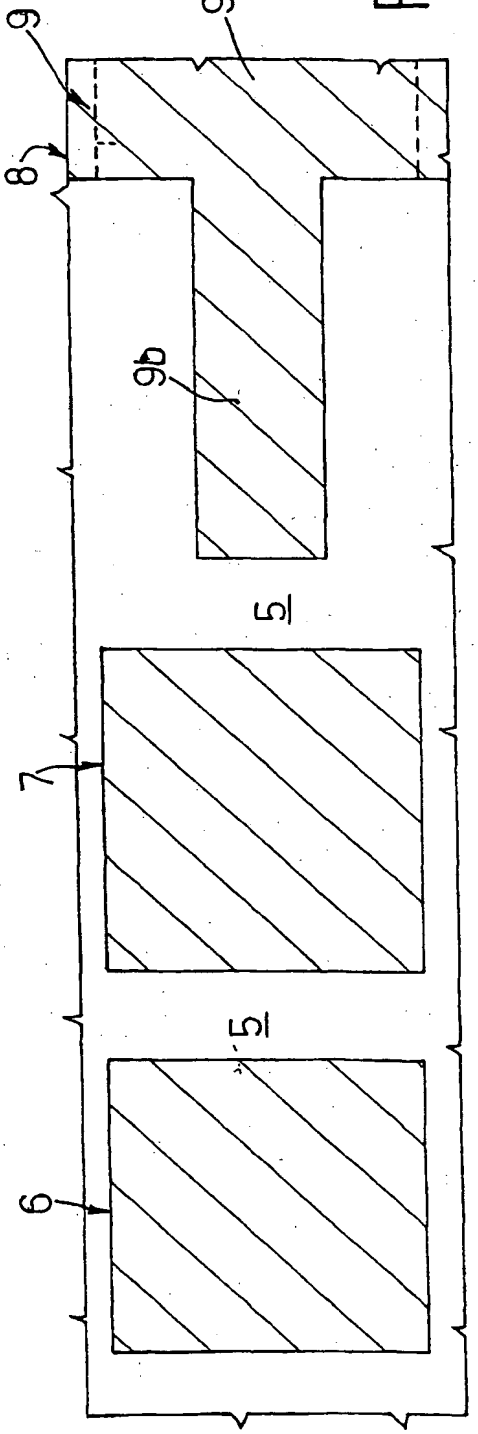


Fig.3

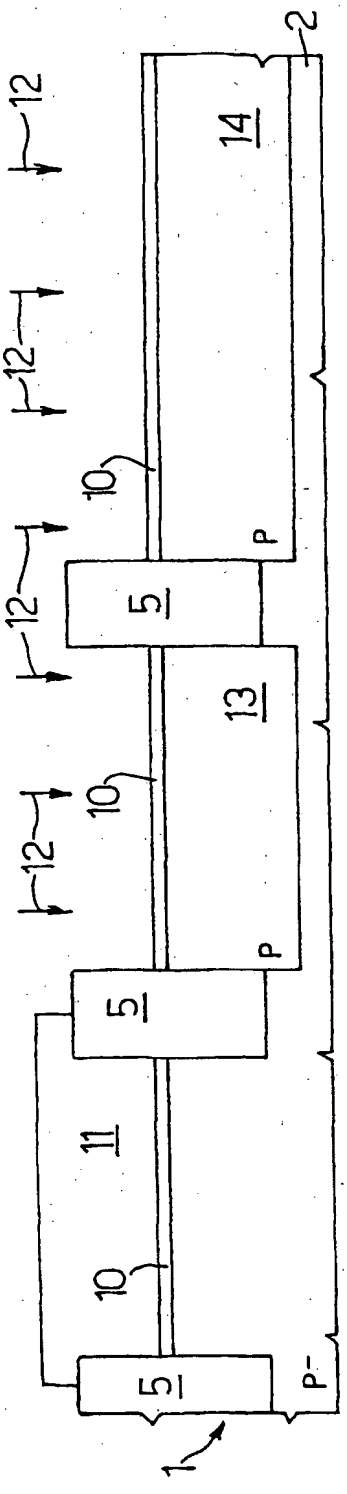


Fig.4

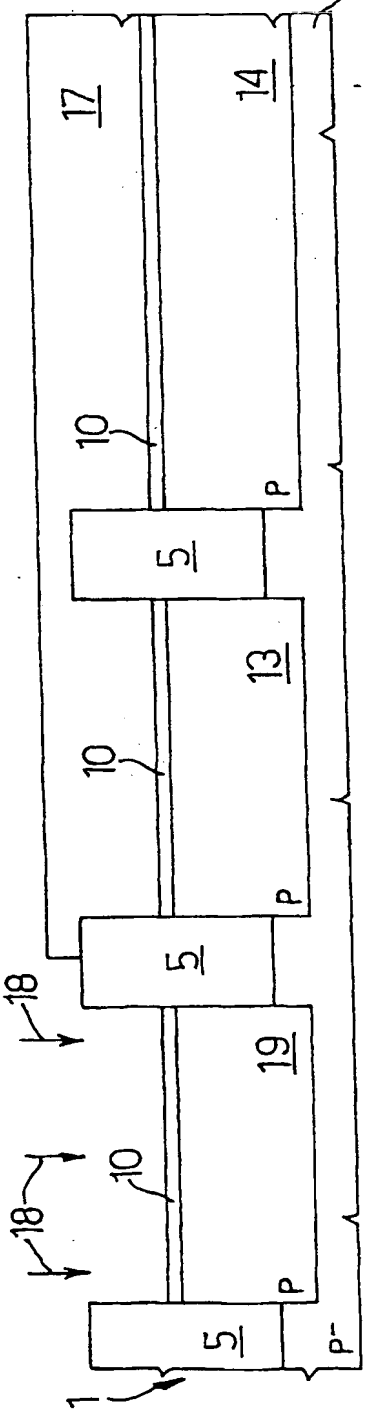

17
14
2
10
P
5
13
10
P
5
18
19
18
10
P
5
1
P-

Fig.5

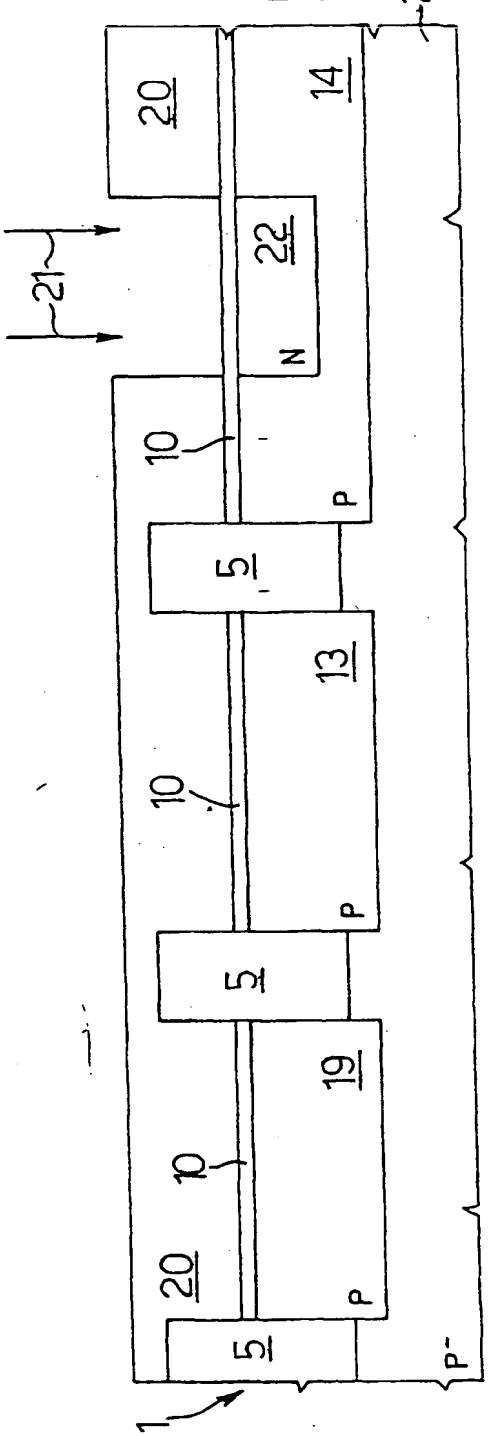

20
14
2
21
22
N
10
P
5
13
10
P
5
19
10
20
P
5
1
P-

Fig.6

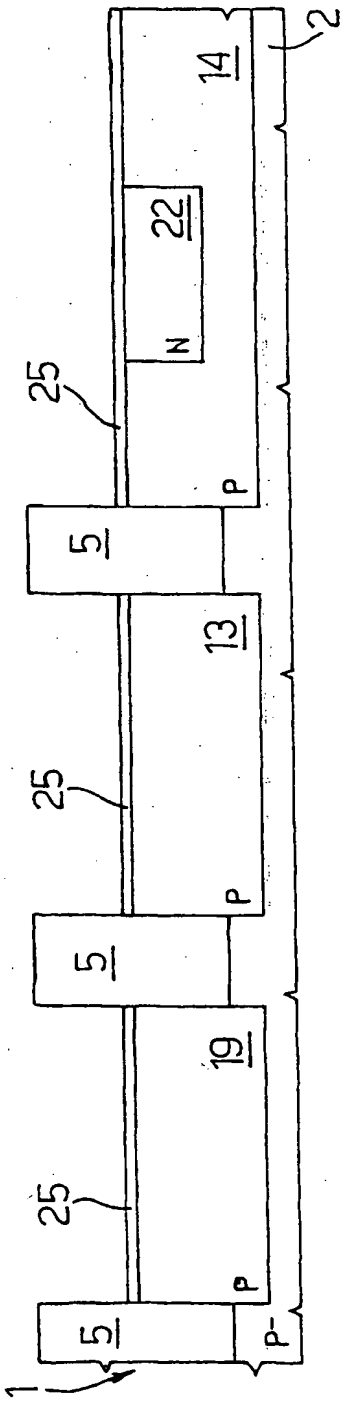


Fig.7

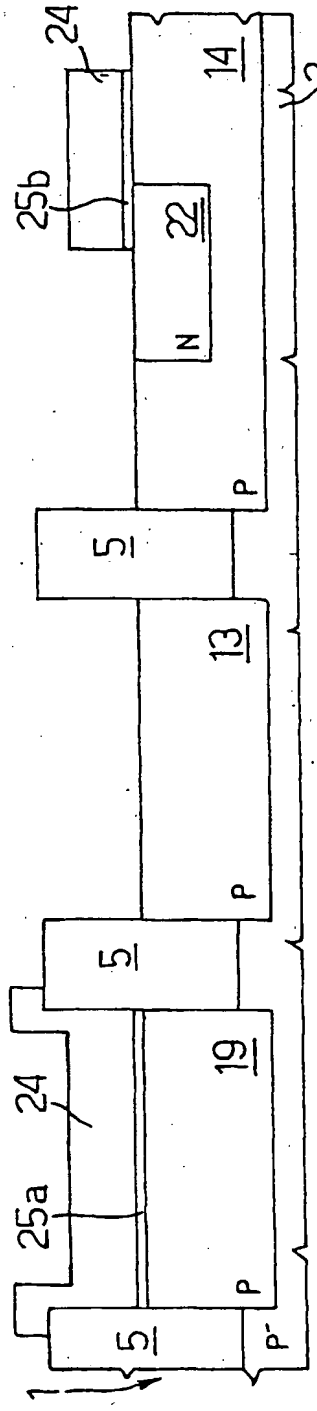


Fig.8

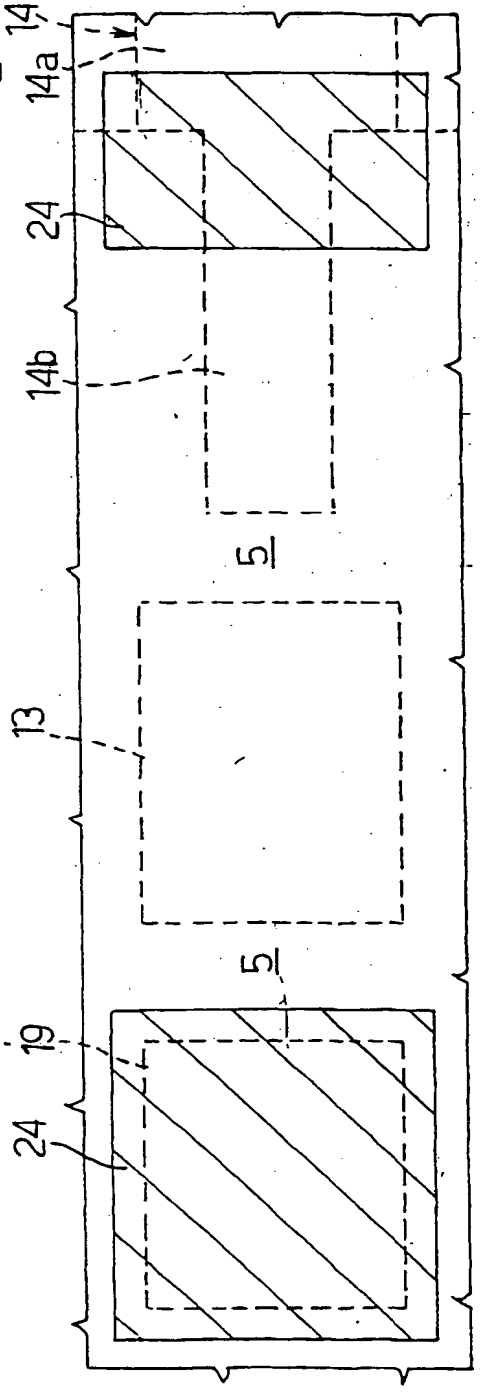


Fig.9

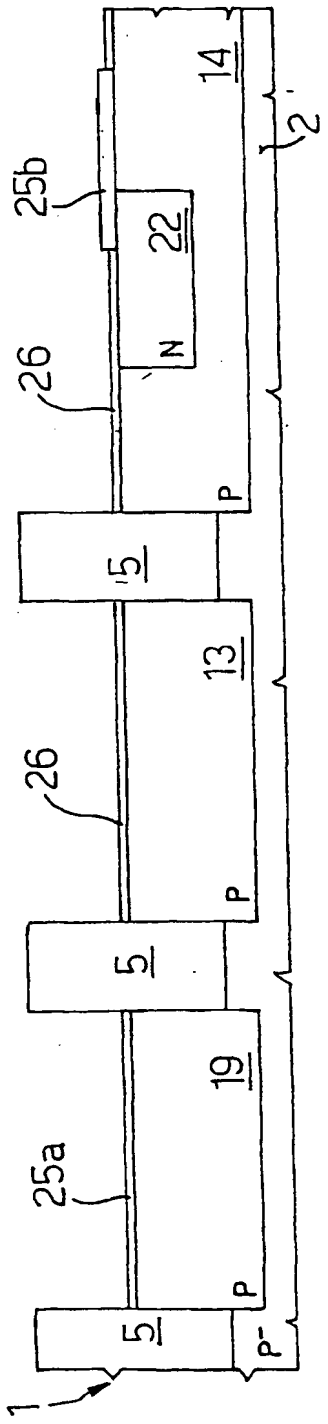

1
5
P-
25a
19
P
26
13
5
25b
22
N
14
2

Fig.10

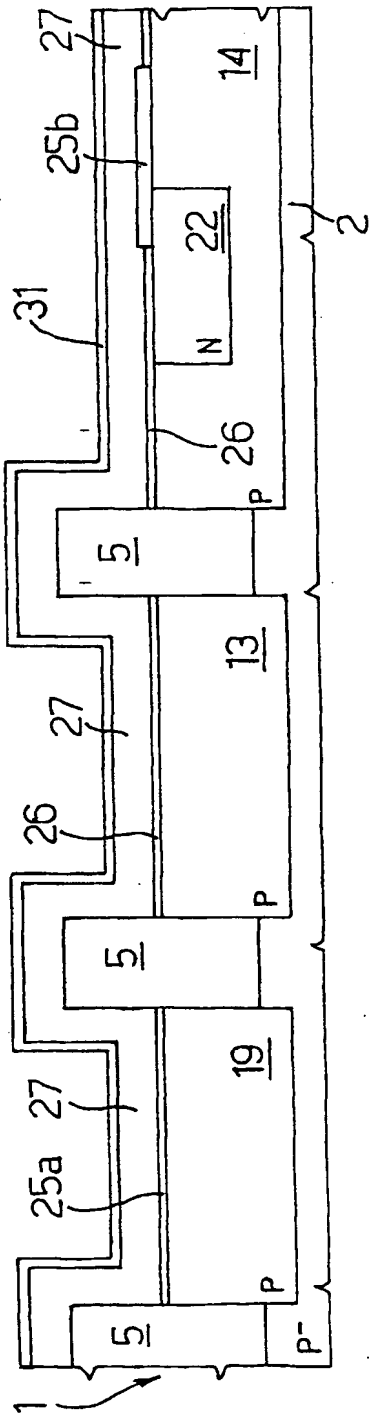

1
5
P-
25a
27
19
P
26
13
5
31
25b
22
N
14
2

Fig.11

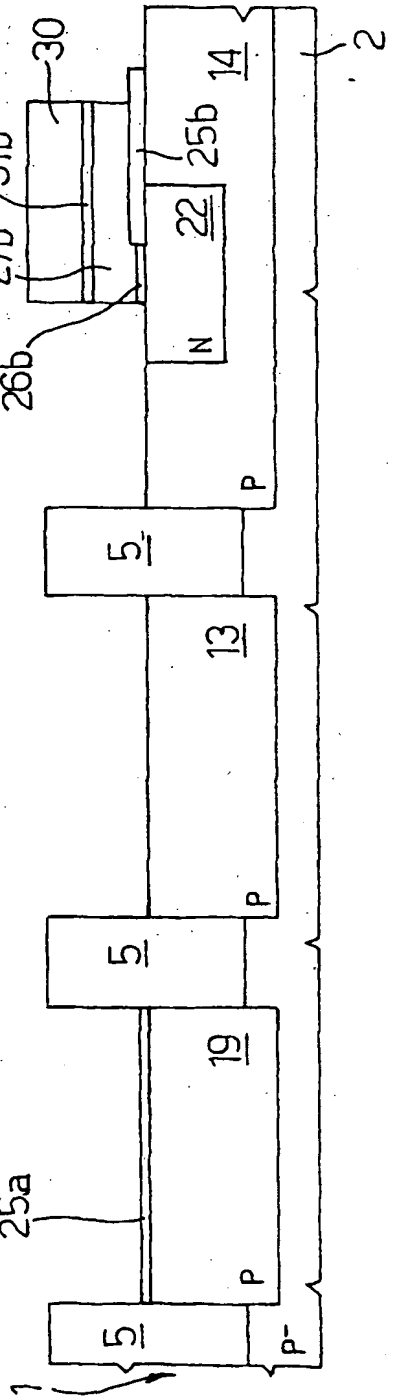


Fig.12

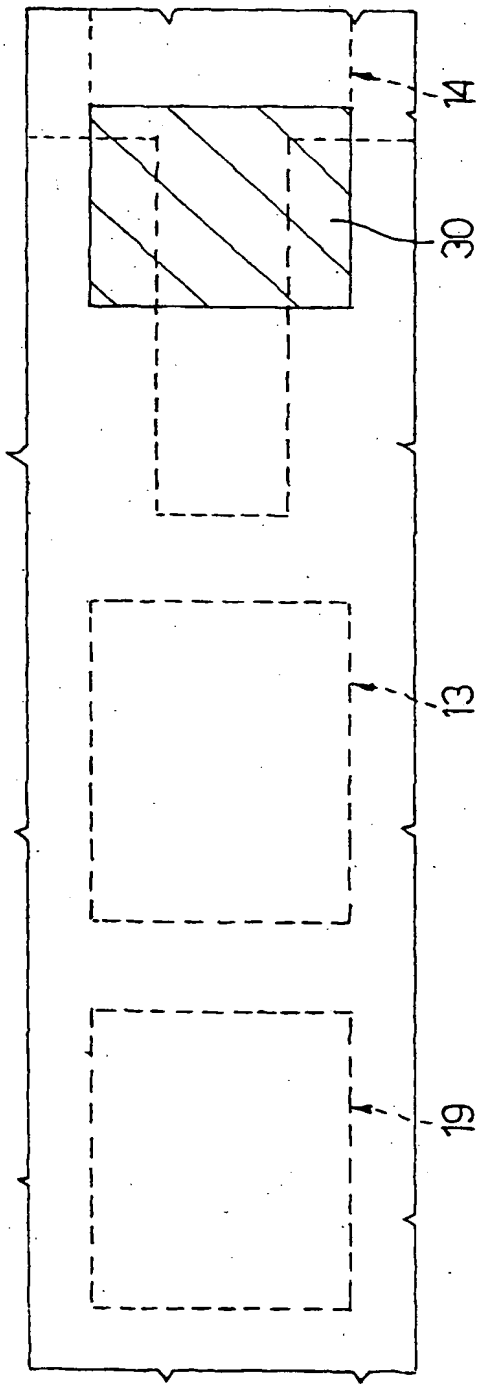


Fig.13

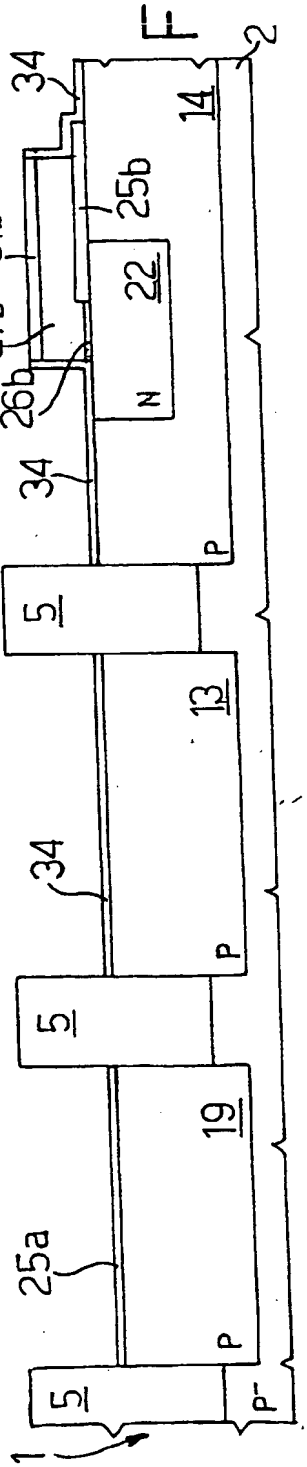


Fig.14

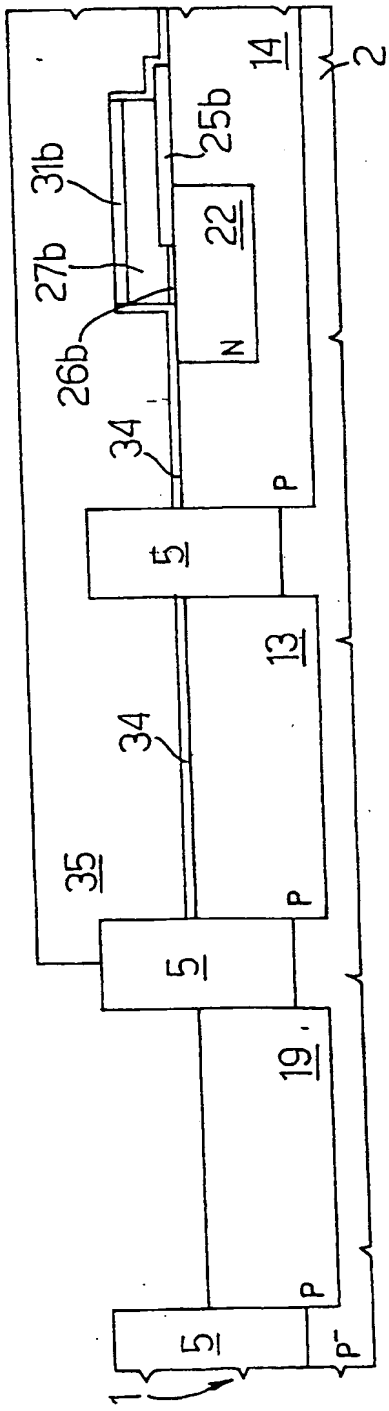


Fig.15

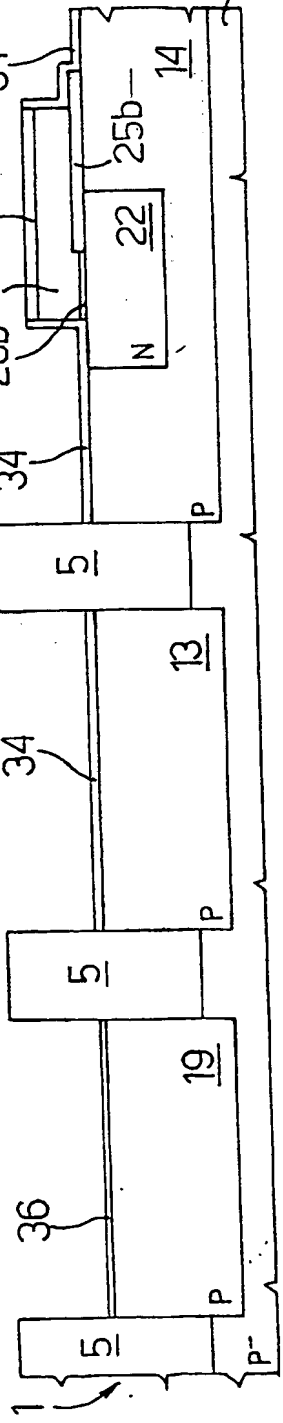


Fig.16

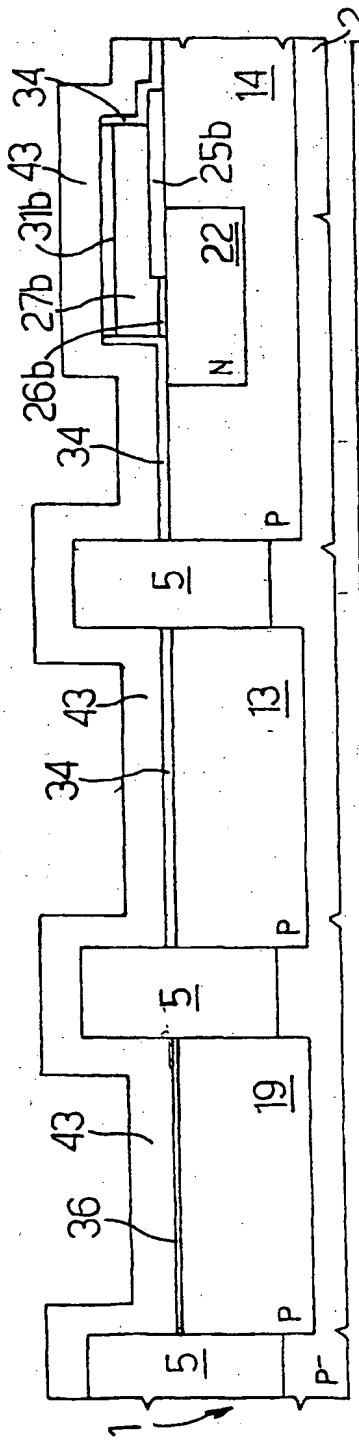


Fig.17

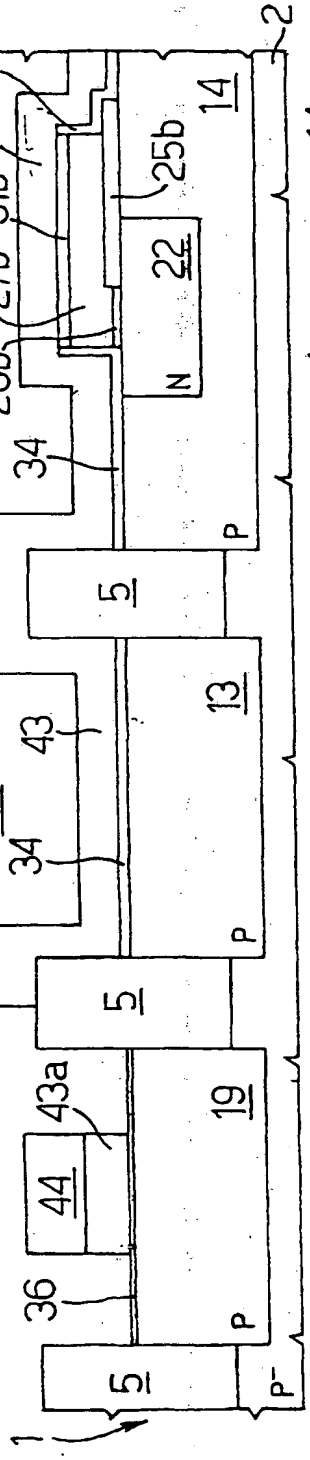
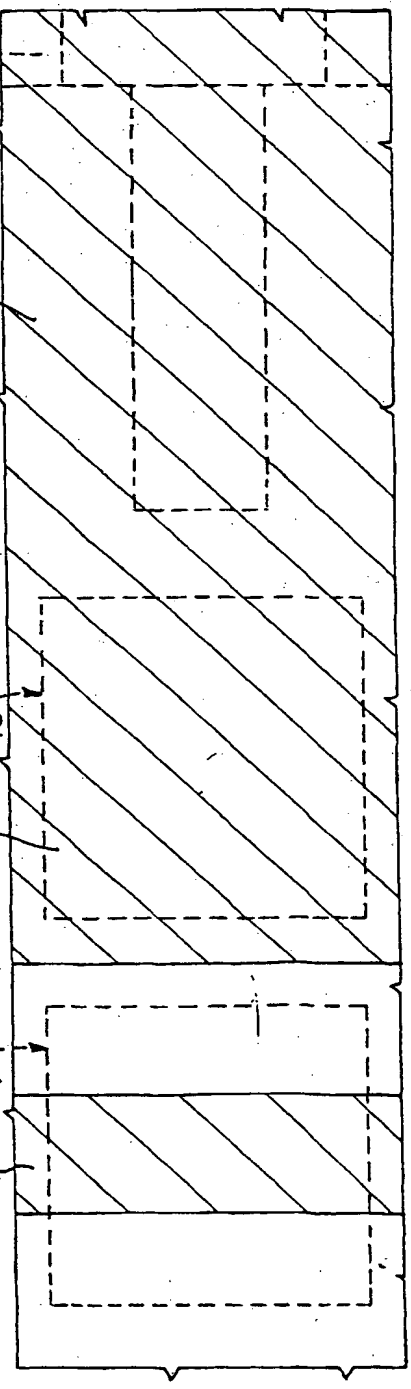


Fig.18



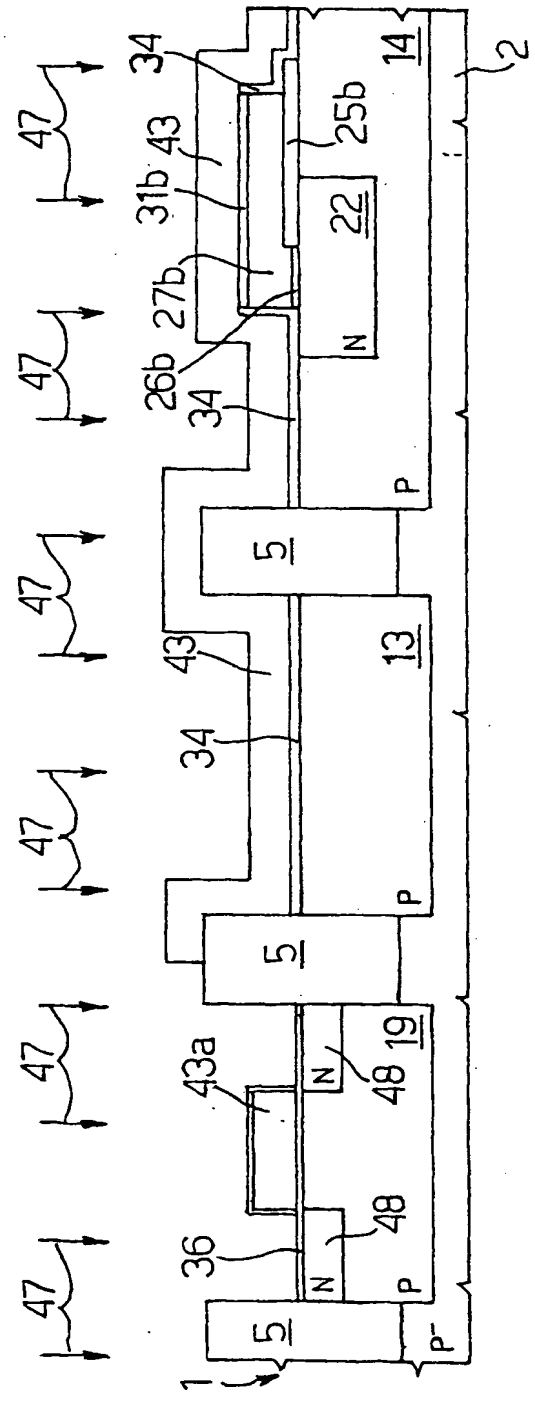

47
34
43
31b
27b
26b
34
25b
14
22
N
2
5
P
43
13
34
5
P
43a
N
48
19
36
N
48
P
5
P⁻
1

Fig.19

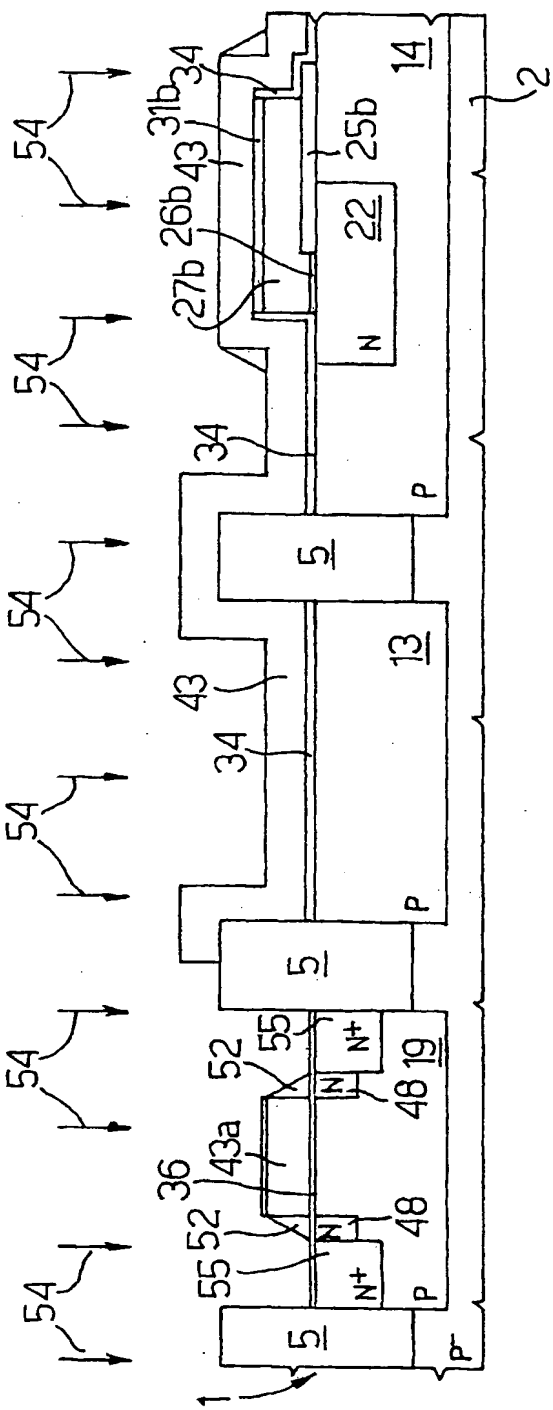

54
34
31b
43
26b
27b
25b
14
22
N
2
5
P
43
13
34
5
P
52
55
N+
N
48
19
43a
36
52
55
N
48
N+
P
5
P⁻
1

Fig.20

Fig.21

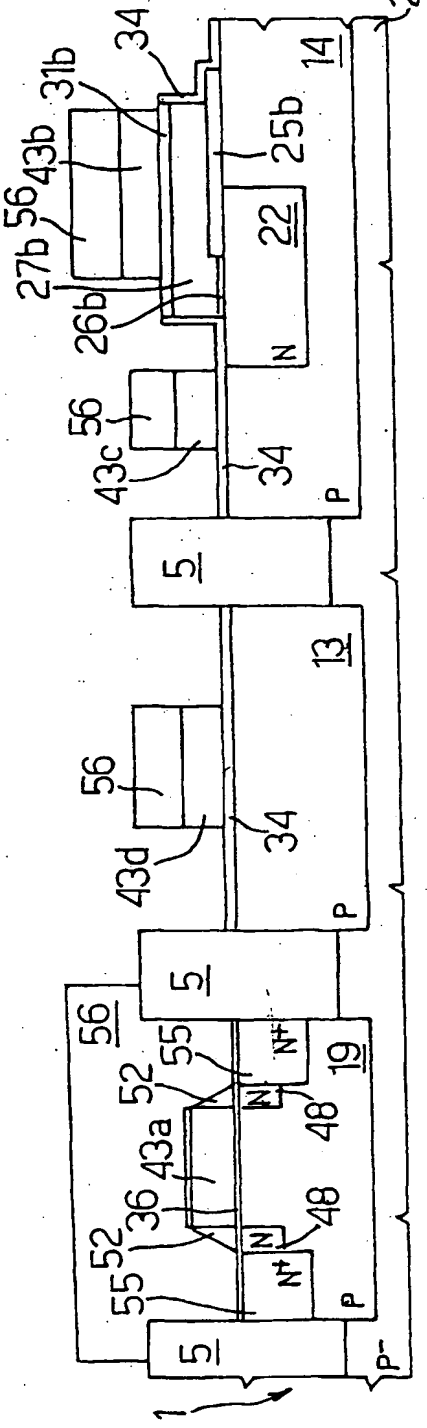
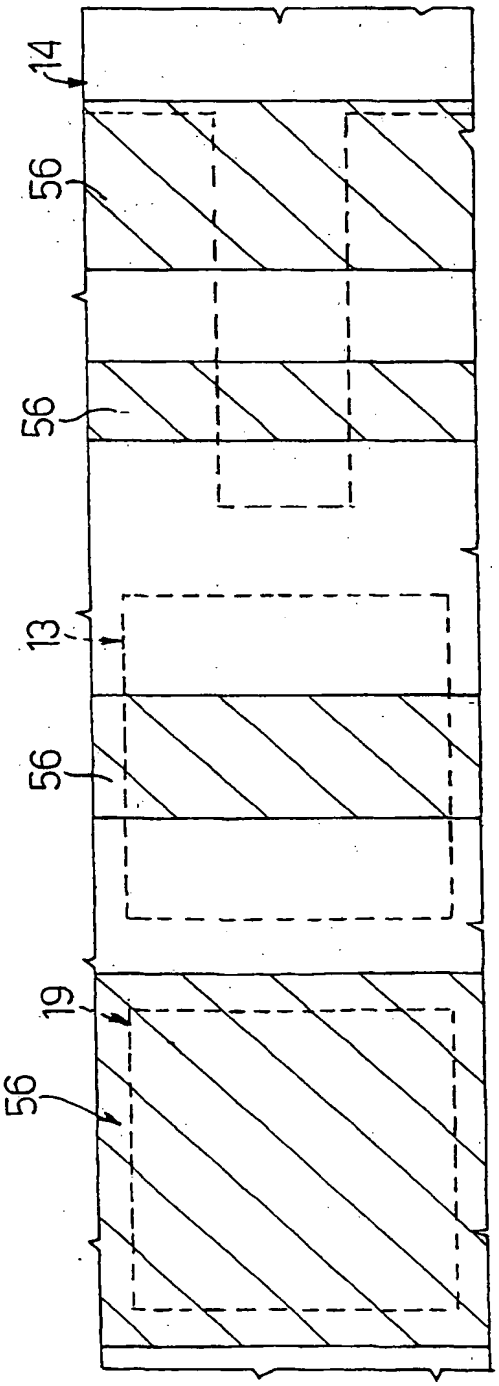

1
2
5
13
14
19
22
25b
26b
27b
31b
34
36
43a
43b
43c
43d
48
52
55
56
N
N+
P
P-

Fig.22


13
14
19
56

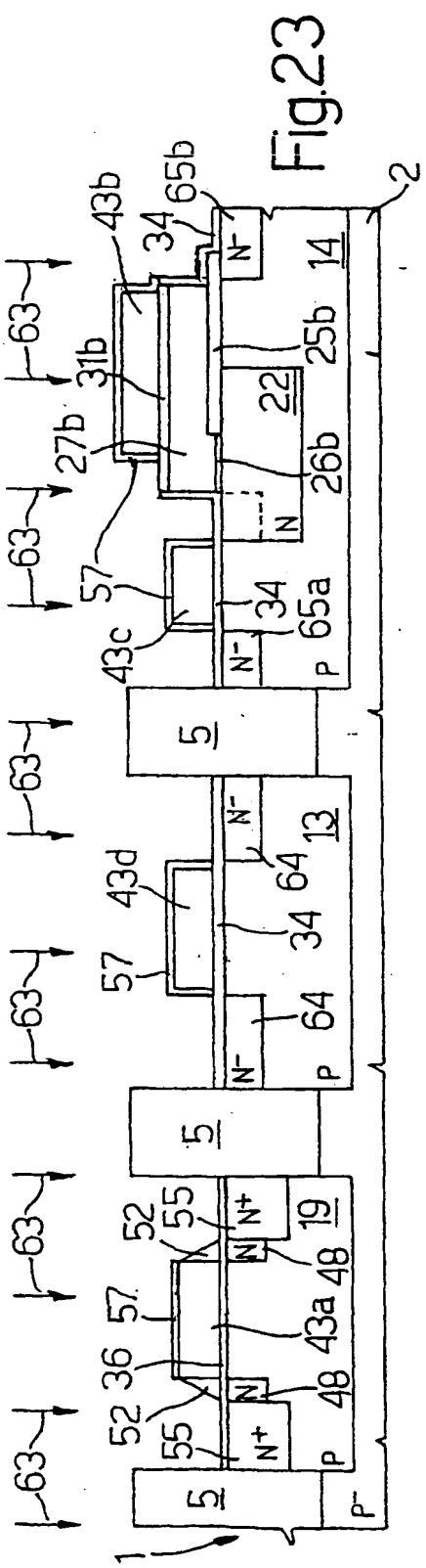

63
63
63
63
63
63
43b
65b
34
31b
27b
57
43c
43d
36
43a
52
55
48
64
70
72
N+
N-
N
P
P-
1
2
5
13
14
19
22
25b
26b
65a

Fig.23

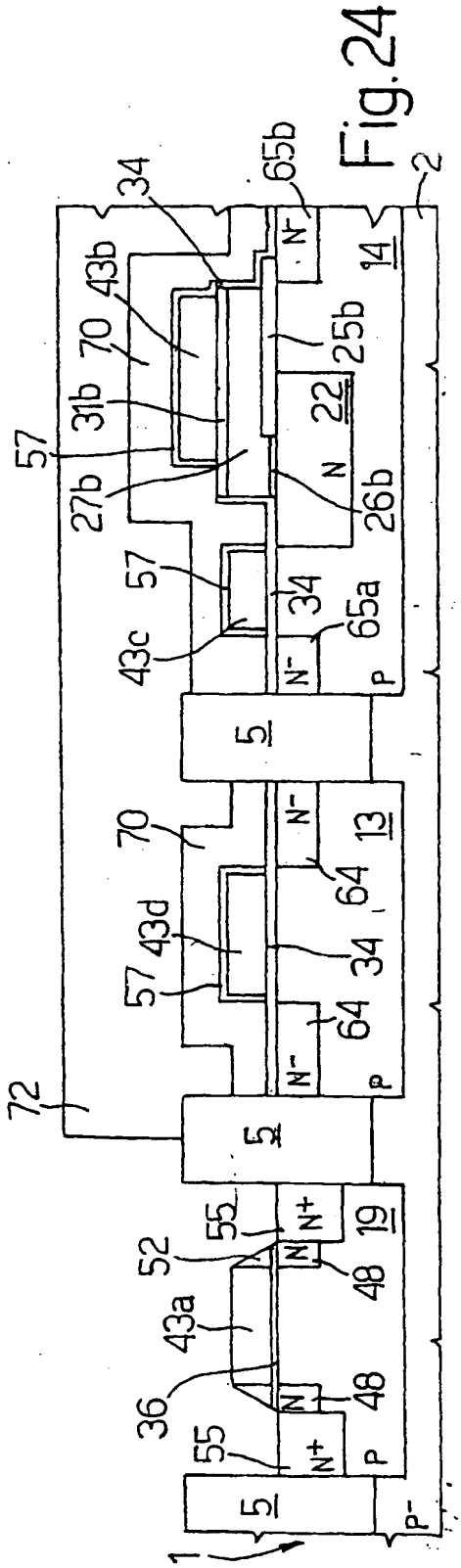

57
34
65b
43b
70
31b
27b
25b
22
26b
43c
65a
5
13
14
19
43d
64
43a
36
52
55
48
72
N+
N-
N
P
P-
1
2

Fig.24

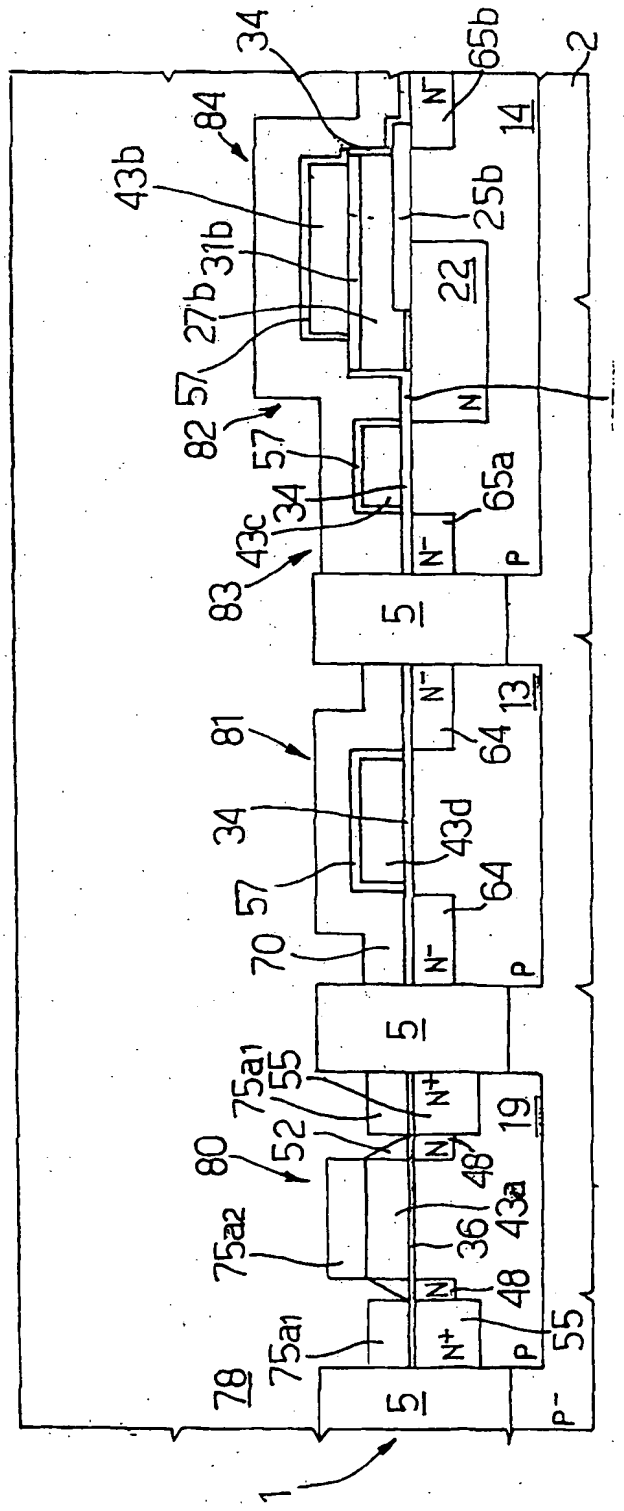

34
65b
2
84
N-
14
43b
25b
31b
22
27b
57
26b
82
57
34
65a
43c
N-
P
83
5
N-
13
81
64
34
43d
64
57
N-
P
70
5
75a1
55
N+
19
80
52
N
48
43a
75a2
36
N
48
N+
P
55
75a1
78
5
P-
1

Fig. 25

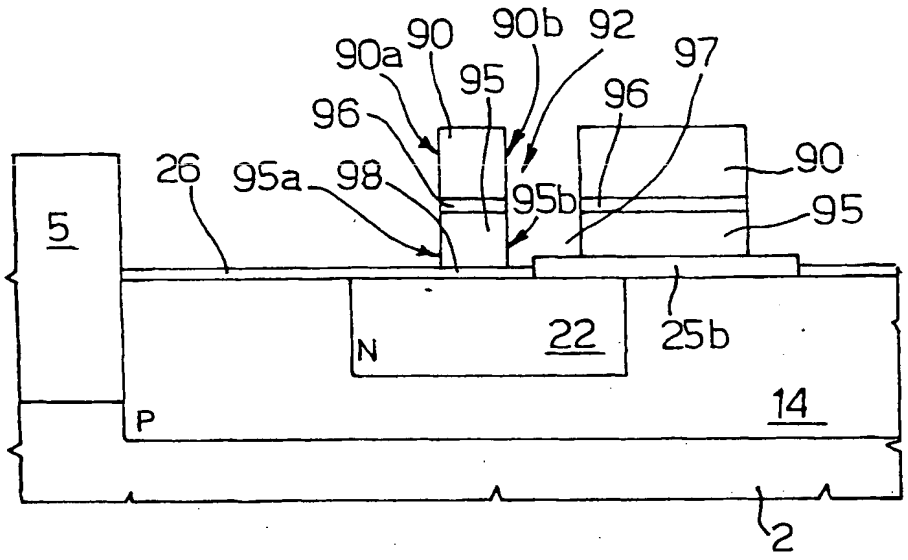

90a
90
90b
92
97
95
96
96
26
95a
98
95b
90
95
5
N
22
25b
14
P
2

Fig.26

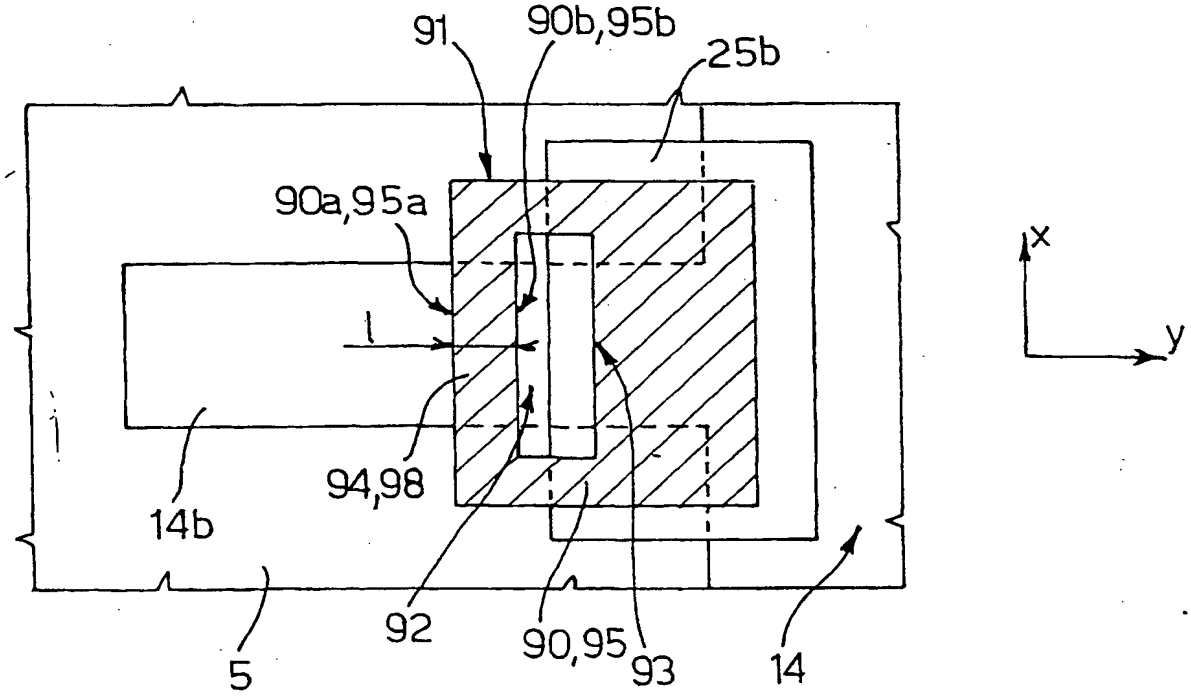

91
90b,95b
25b
90a,95a
l
94,98
14b
92
90,95
93
14
5
x
y

Fig.27

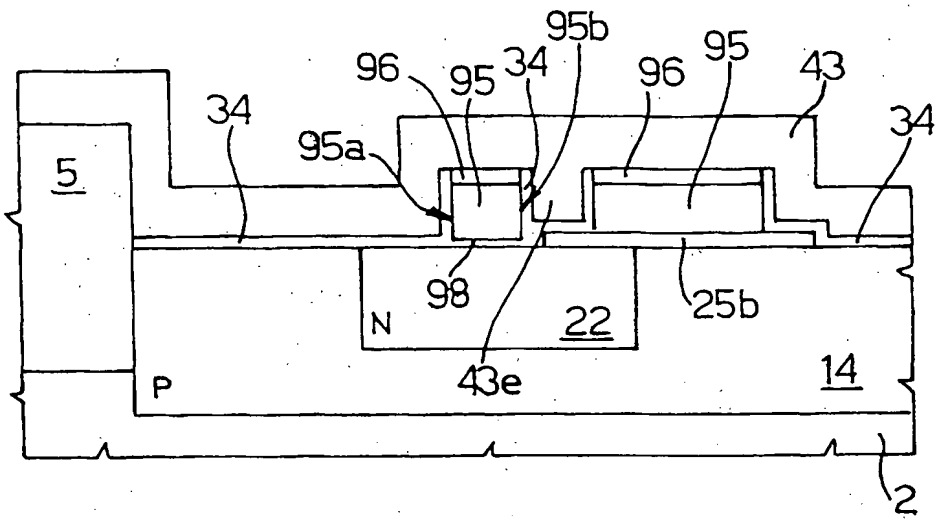

95b
96
95
34
96
95
43
34
95a
34
5
98
N
22
25b
43e
P
14
2

Fig. 28

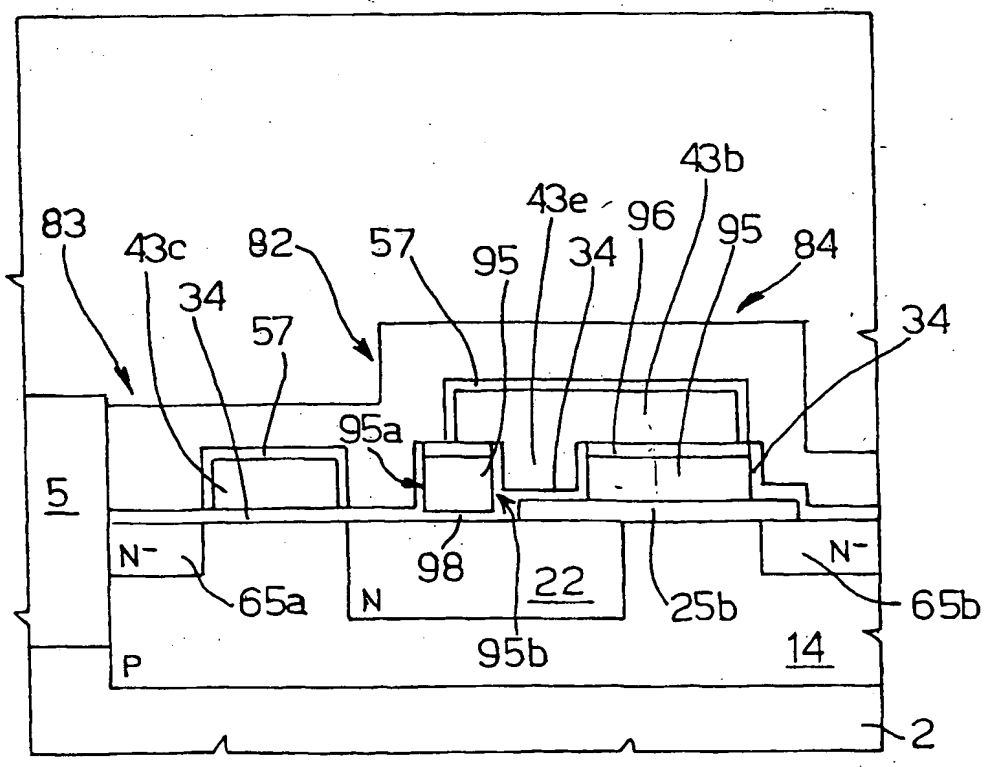

43b
43e
96
95
84
83
43c
82
57
95
34
34
57
34
95a
5
N⁻
98
22
N⁻
65a
N
25b
65b
95b
P
14
2

Fig. 29

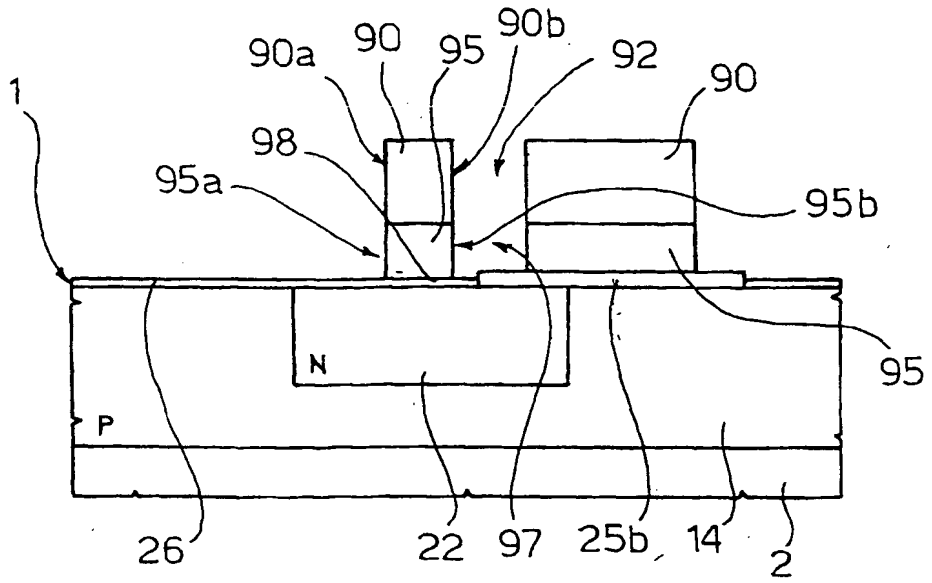

1
90a
90
95
90b
92
90
98
95a
95b
95
N
P
26
22
97
25b
14
2

Fig.30

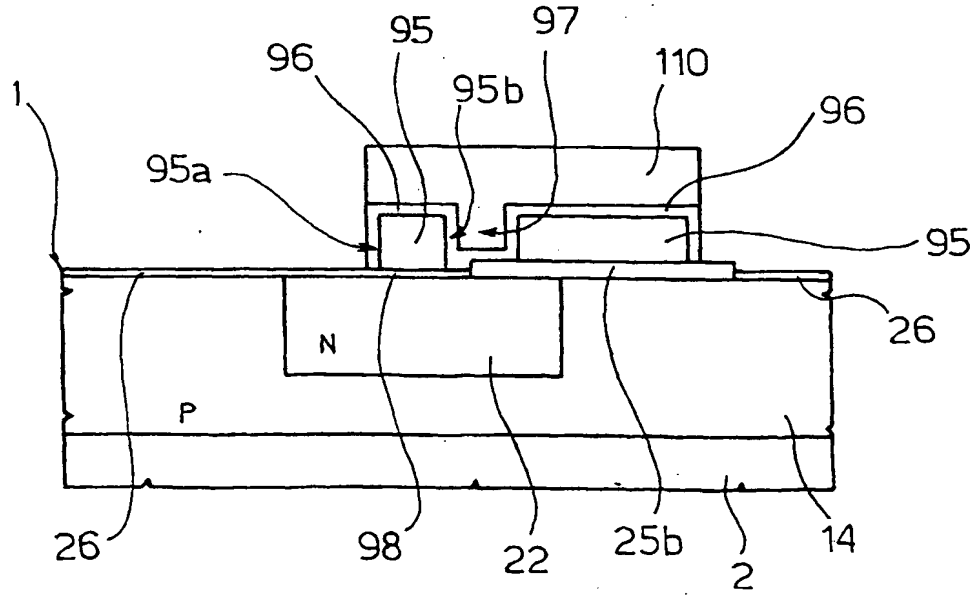

1
96
95
97
110
95b
96
95a
95
N
26
P
26
98
22
25b
2
14

Fig.31

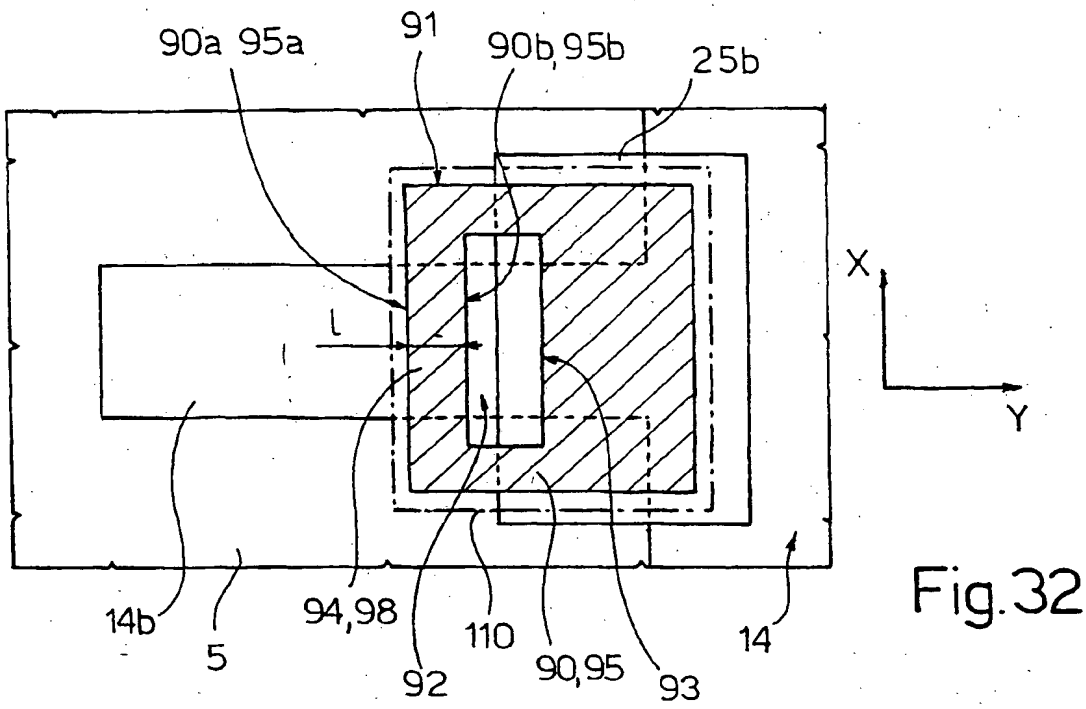

90a 95a
91
90b 95b
25b
X
Y
L
14b
5
94,98
92
110
90,95
93
14

Fig.32

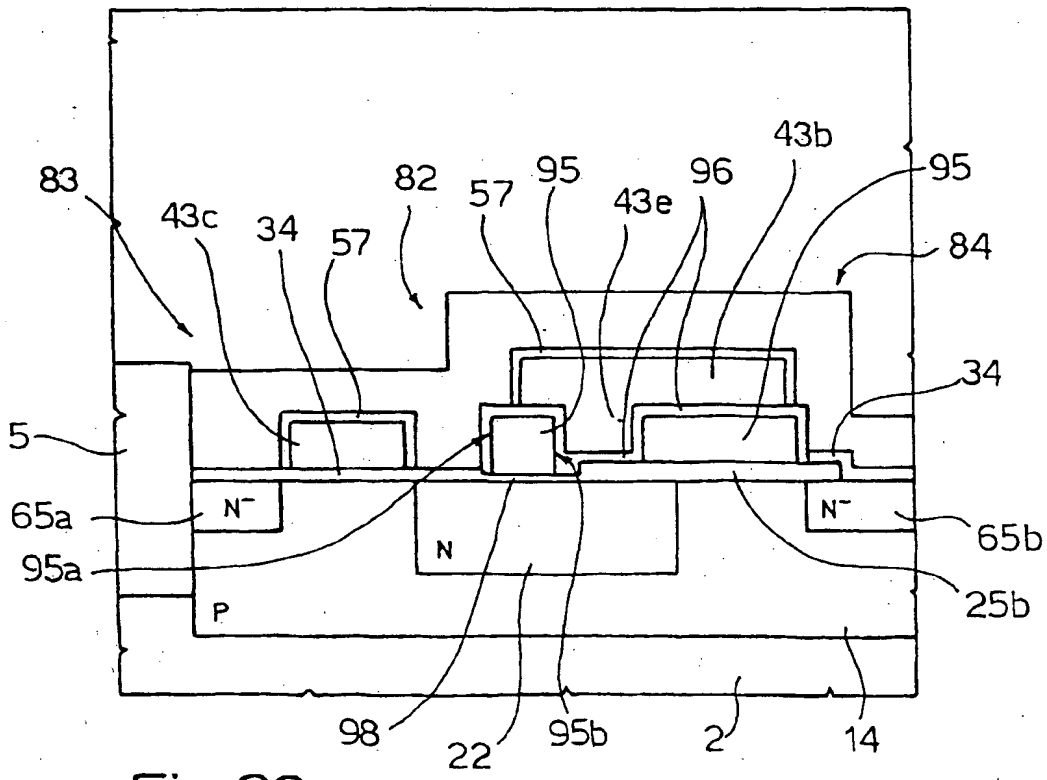

83
43c
34
57
82
57
95
43e
96
43b
95
84
34
5
65a
N⁻
95a
N
N⁻
65b
P
25b
98
22
95b
2
14

Fig.33

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0346

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	US 4 794 562 A (ASANO MASAMICHI ET AL) 27 December 1988 (1988-12-27) * column 5, line 39 - column 7, line 56; figures *	1-4,8-11	H01L27/115 H01L29/788 H01L21/8247
Y	HART M J ET AL: "A BACK - BIASED 0.65 UM LEFFN CMOS EEPROM TECHNOLOGY FOR NEXT - GENERATION SUB 7 NS PROGRAMMABLE LOGIC DEVICES" MICROELECTRONIC ENGINEERING,NL,ELSEVIER PUBLISHERS BV., AMSTERDAM, vol. 15, no. 1 / 04, page 613-616 XP000292796 ISSN: 0167-9317 * the whole document *	1-4,8-11	
A	US 4 688 078 A (HSEIH NING) 18 August 1987 (1987-08-18) * column 10, line 21 - column 13, line 68; figures 8B,17 *	1,5-7,9	
A	US 5 066 992 A (WU TSUNG-CHING ET AL) 19 November 1991 (1991-11-19) * the whole document *	1-11	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
A	EP 0 811 983 A (SGS THOMSON MICROELECTRONICS) 10 December 1997 (1997-12-10) * column 3, line 23 - column 4, line 30; figures *	1-11	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	10 November 1999	Blackley, W

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 83 0346

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

10-11-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4794562 A	27-12-1988	JP 1874497 C	26-09-1994
		JP 5086075 B	09-12-1993
		JP 63084168 A	14-04-1988
US 4688078 A	18-08-1987	CA 1204862 A	20-05-1986
		EP 0105802 A	18-04-1984
		JP 59112657 A	29-06-1984
US 5066992 A	19-11-1991	NONE	
EP 0811983 A	10-12-1997	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82